



ID-FAST



Development, application and validation of accelerated durability tests for stacks

S. Escribano, F. Micoud, N. Mariage, L. Guétaz (CEA)
A. Casalegno, A. Baricci, E. Colombo (Polimi)
M. Schmid, F. Wilhelm (ZSW)

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Online in the Framework of the EFC21



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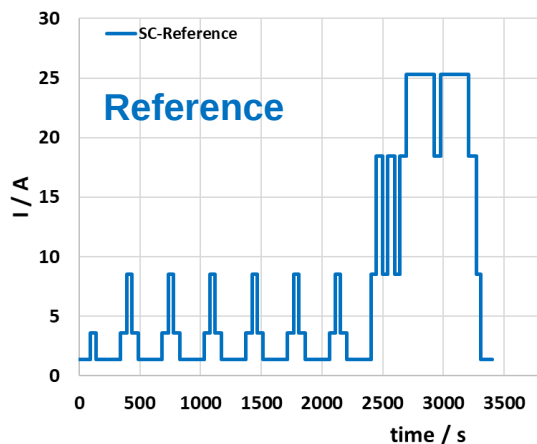
ID-FAST



An AST approach applied on F stacks

- ❑ Starting from the reference load cycle profile
→ Increase intensity of voltage / current stressors to accelerate performance loss degradation
- ❑ Developed first using single cell (25 cm^2 - single serpentine)
 - Simplified procedure adapted/transferable to most of test benches and cell designs

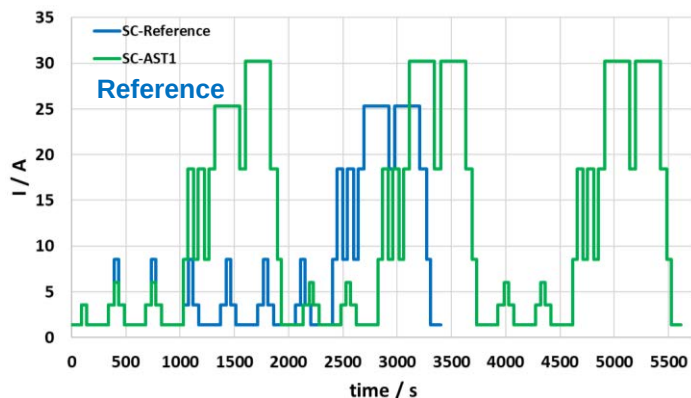
Reference SC load cycles



- Initial adjusted load profile to nominal conditions of the targeted stack
 - $i_{\max} = 1 \text{ A/cm}^2$ (0.64 V)
 - Fixed temperature 80°C - RH 50/50% - 1.5 bara
 - No stops included (operational hours preferred)

- ❑ More intensive load cycles (i.e. voltage cycles)
 - Increase the current range and voltage range
 - lower minimum and higher maximum
 - Change the frequency of low and high current period

First modified version AST



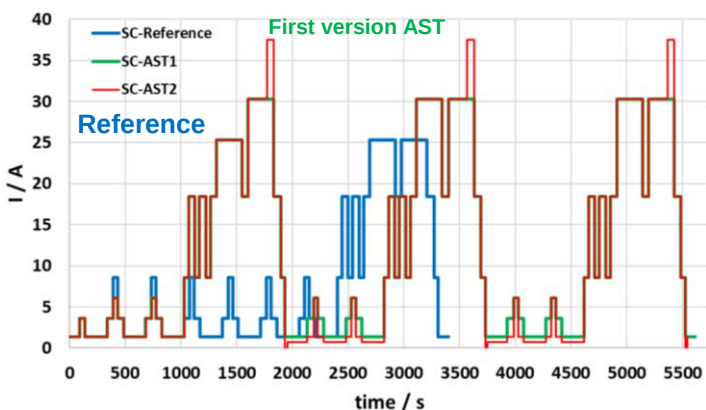
First attempt AST SC profile

- Modifications
 - $i_{\max} = 1.2 A/cm^2$ (0.6 V)
 - More frequent transitions between low and high power phases
 - Relatively more time at high power
- *Note: for development, some current steps kept identical as reference for comparisons between different cases*

- ❑ More intensive load cycles (i.e. voltage cycles)
 - Increase the current range and voltage range
- ❑ → lower minimum and higher maximum
- Change the frequency of low and high current period

Second version AST

More time + exacerbated min & max currents

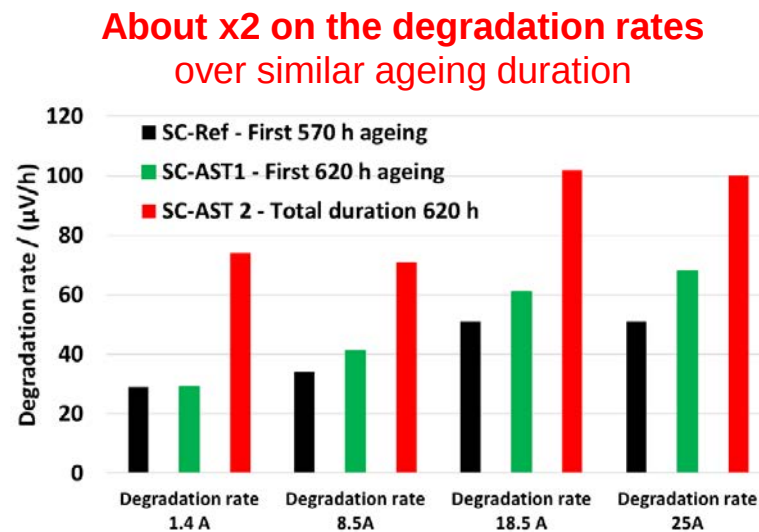
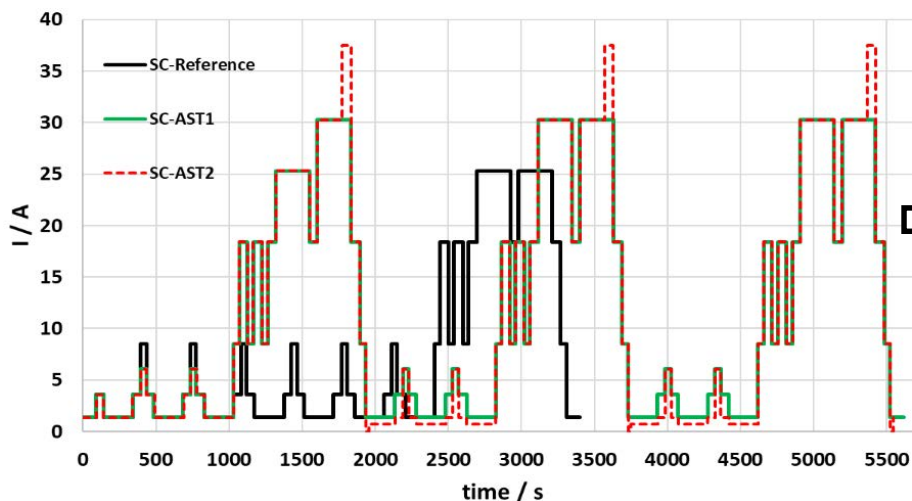


Second attempt AST SC profile

- Modifications
 - $i_{\max} = 1.5 \text{ A/cm}^2$ as additional peak (0.5 V)
 - More frequent transitions between low and high power phases
 - Relatively more time at high power
 - Addition of short OCV steps (after peak)
- As additional stressor identified on specific tests (two current steps AST)
- *Note: for development, some current steps kept identical as reference for comparisons between different cases*

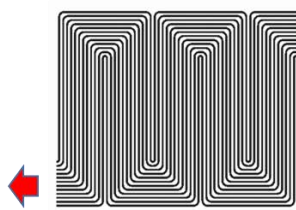
- ❑ More intensive load cycles (i.e. voltage cycles)
 - Increase the current range and voltage range
- ❑ → lower minimum and higher maximum
 - Change the frequency of low and high current period

Application on ~600 hours for the 3 load profiles (25 cm² - SC with CCM A)
➔ Increased degradation rates confirmed at single cell level

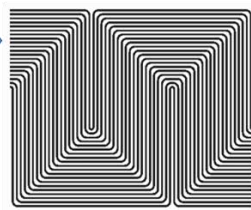


- AST methodology adapted for stack level (220 cm² - open design)

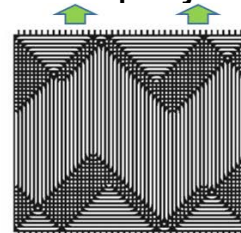
Technology identified for the project following historical use in Kangoo cars and previous FCH-JU projects



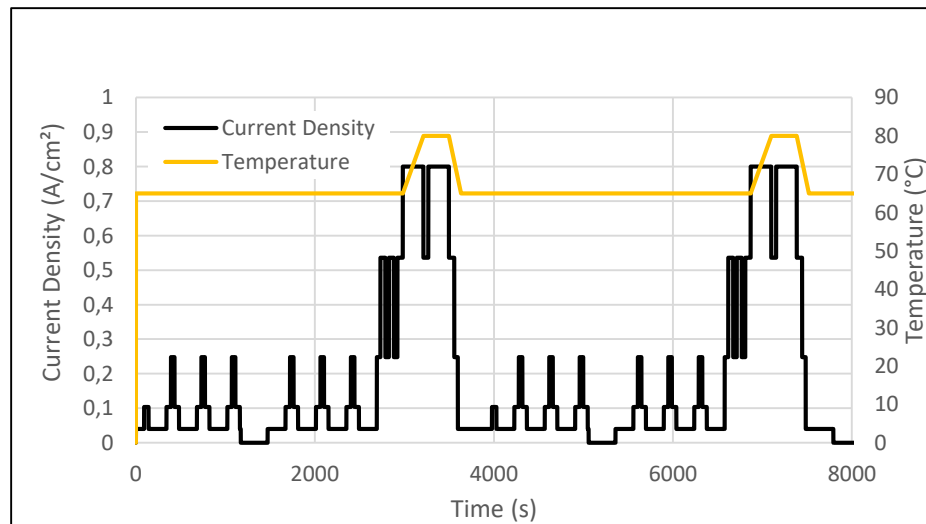
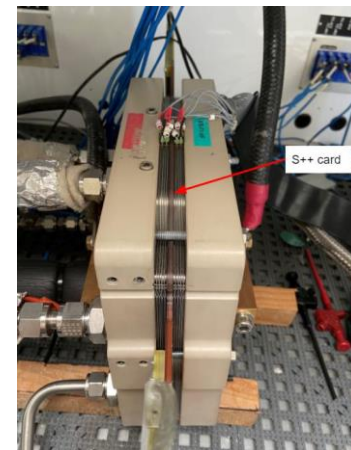
H₂



Air



Coolant

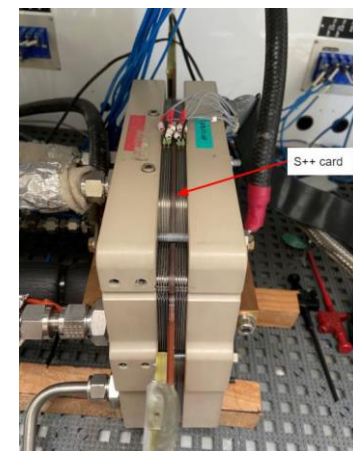
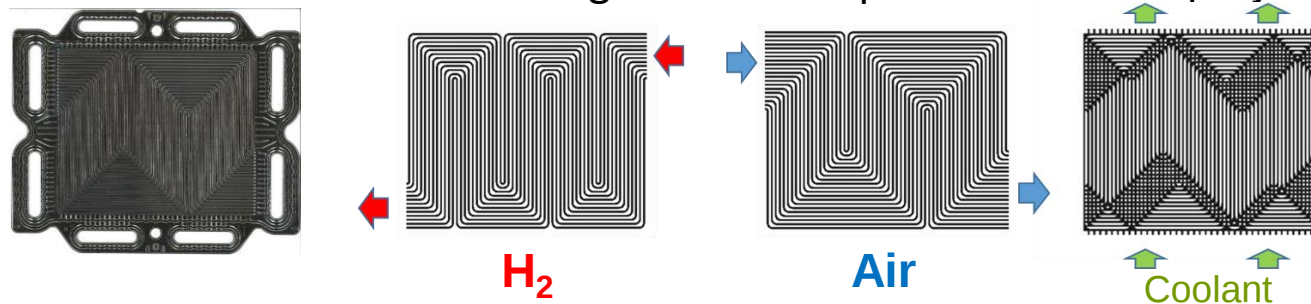


ID-FAST drive cycles specifications

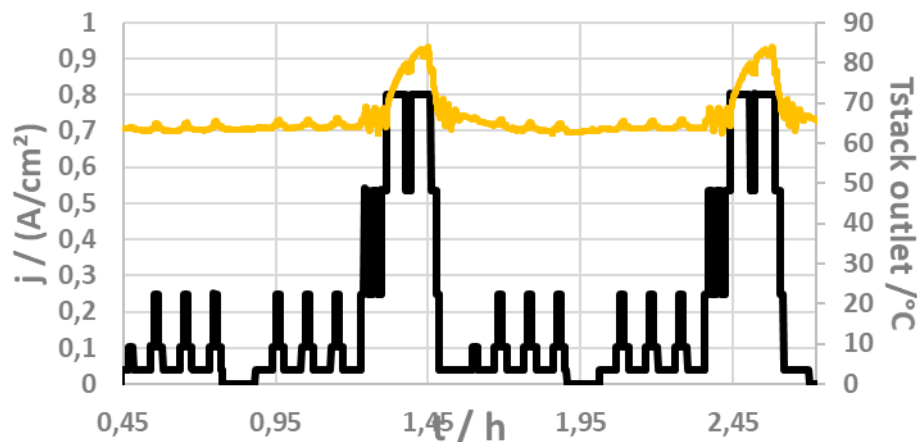
- Adapted parameters for F-design
 - Load profile - $i_{\max} = 0.8 \text{ A/cm}^2$ ($\sim 0.6 \text{ V}$)
 - Nominal conditions: 80°C, 50% RH, 1.5 bara, st1.5/2
 - Stops included (short-stops, cold-soak, long stops)
 - Current density distribution (S++[®] segmented device)

- AST methodology adapted for stack level (220 cm² - open design)

Technology identified for the project following historical use in Kangoo cars and previous FCH-JU projects



Example of result

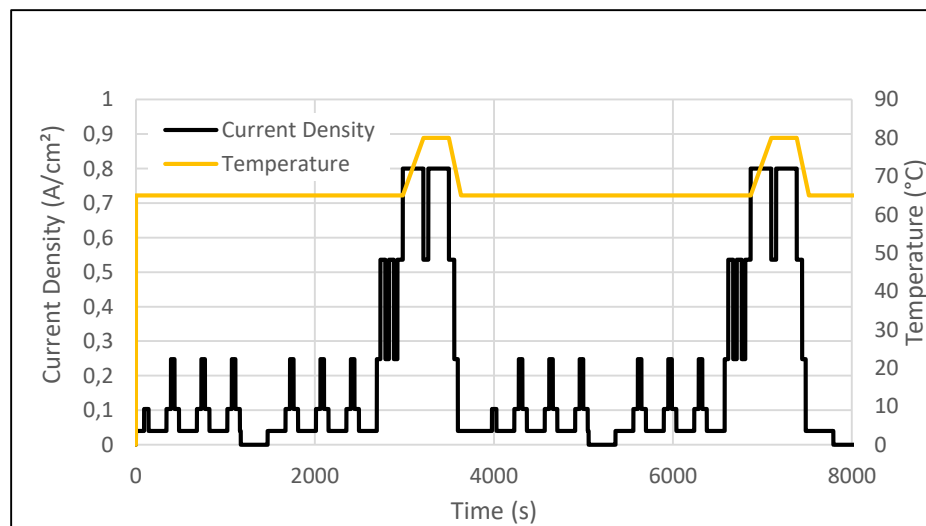
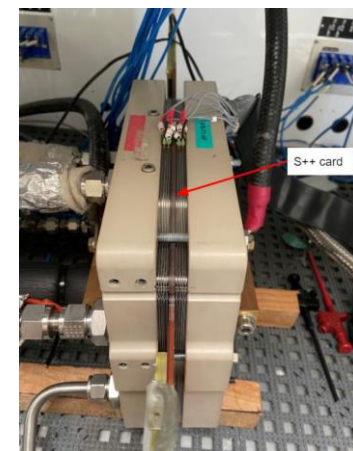
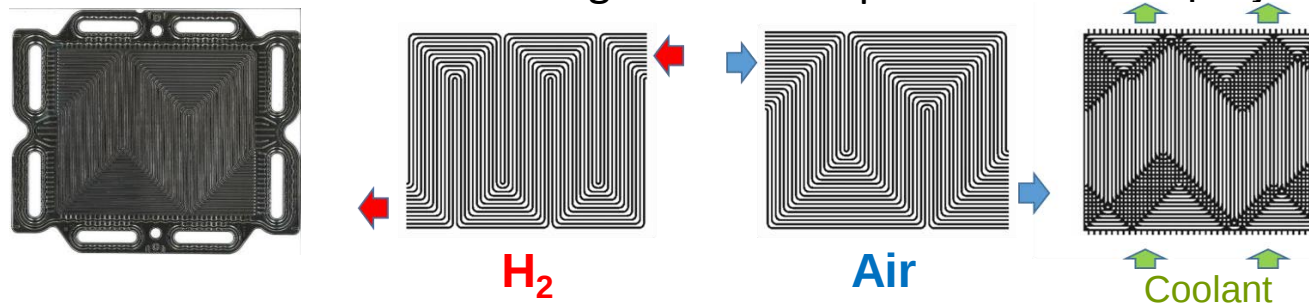


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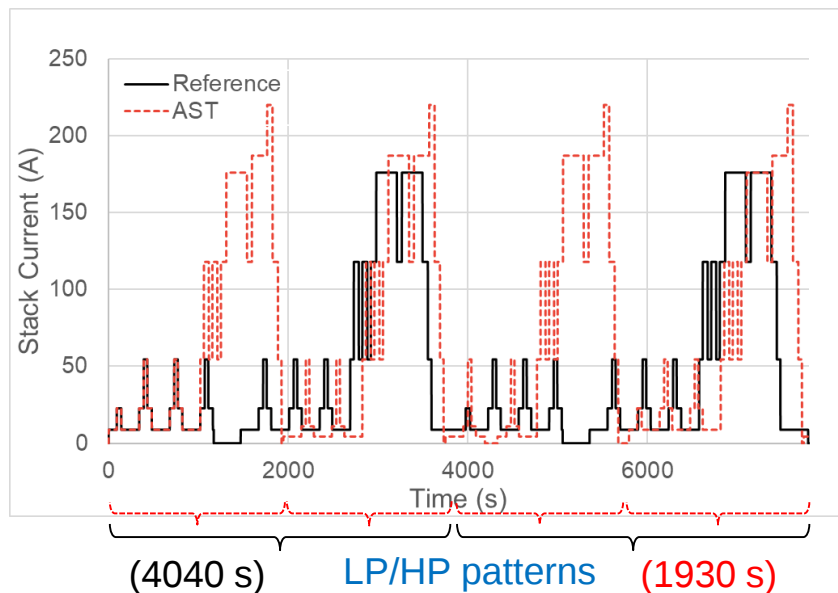
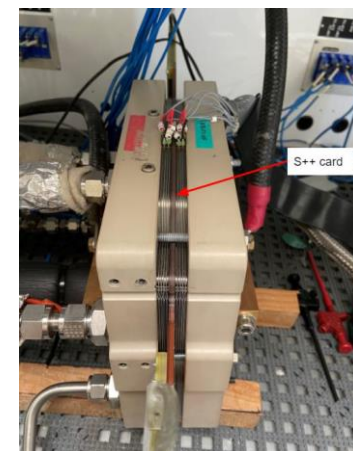
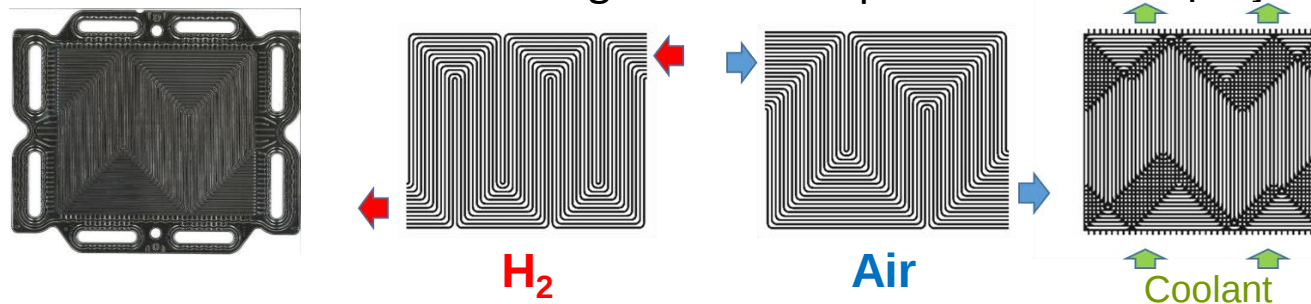
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Direct modification of the ID-FAST drive cycles approach – Stack level

- AST methodology adapted for stack level (220 cm² - open design)

Technology identified for the project following historical use in Kangoo cars and previous FCH-JU projects



Parameters for AST based on 2nd SC case

- Modifications (same stressors as for SC)
 - $i_{\max} = 1 \text{ A/cm}^2$ as additional peak (0.55V)
 - More frequent transitions between low and high power phases
 - Relatively more time at high power
 - Addition of short OCV steps (after peak)

80°C

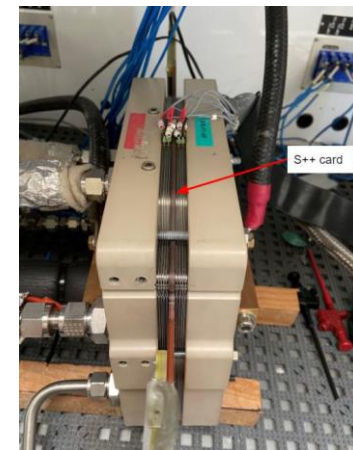
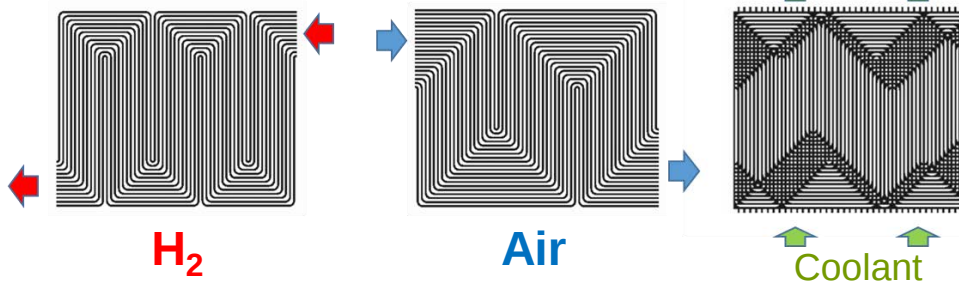
Note: LP/HP patterns can be defined

→ Duration ratio #CyREF/ #CyAST = 1.43

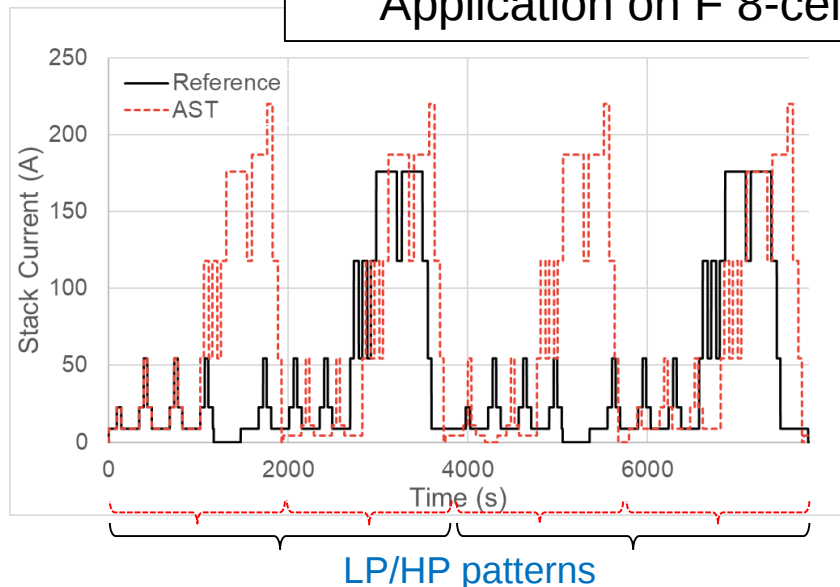
Direct modification of the ID-FAST drive cycles approach – Stack level

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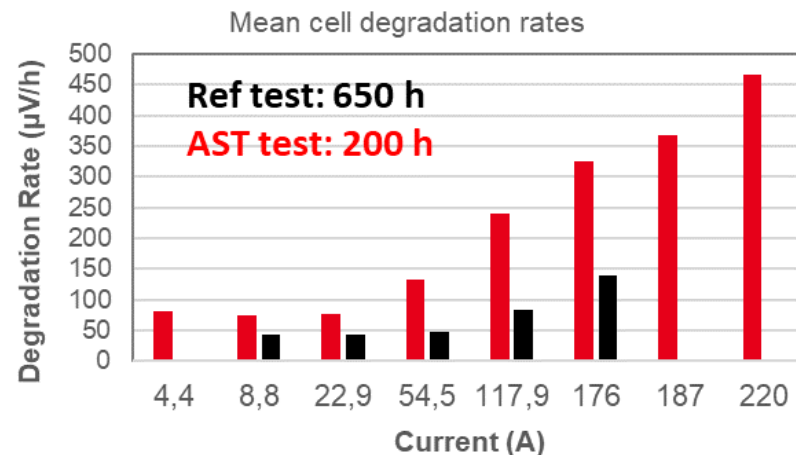
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Application on F 8-cell short stack with CCM A

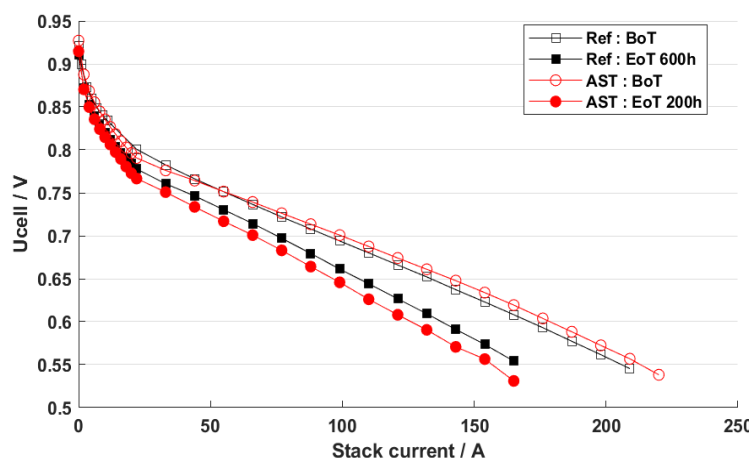
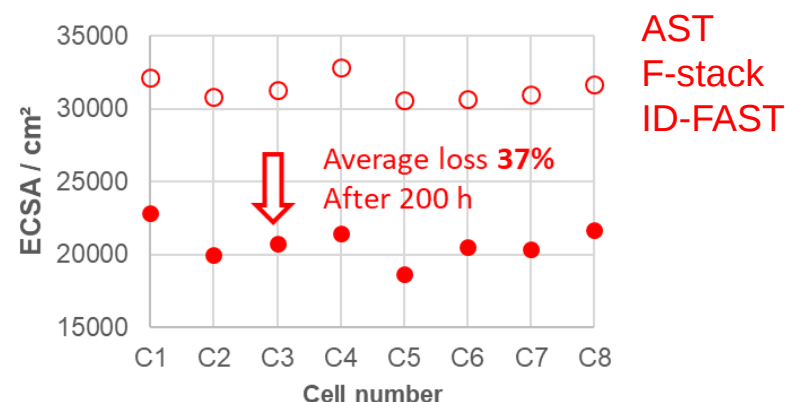
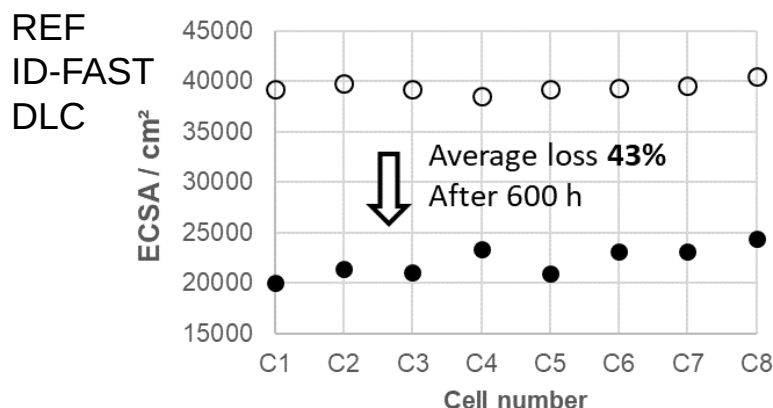


About x3 on the degradation rates
(with EoT performance assessed after 1/3 duration in AST cycles)



- AST methodology adapted for stack level (220 cm² - open design)

Validation of ageing via characterizations at BoT and EoT



- Good qualitative correspondence between REF and AST cases at EoT

- ✓ Similar ECSA loss → among validation criterion of the AST relevance (same range)
- ✓ Similar performance loss on the current range

- Acceleration assessment

- ✓ Voltage loss (mV) AST/REF ~ x1.7 from the i-V curves (at 110 A)
- ✓ Degradation rates (μV/h) AST / REF x5

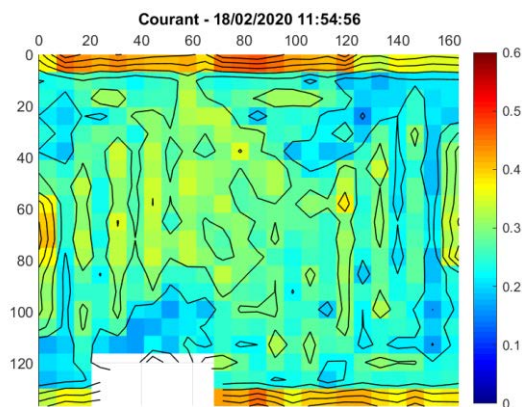
→ Correlation based on the ratio #Cy REF / #Cy AST to reach same EoT performance: ~2,4 (535 cy REF / 220 cy AST)

→ More tests and data analyses needed for refinement and validation.

- AST methodology adapted for stack level (220 cm² - open design)

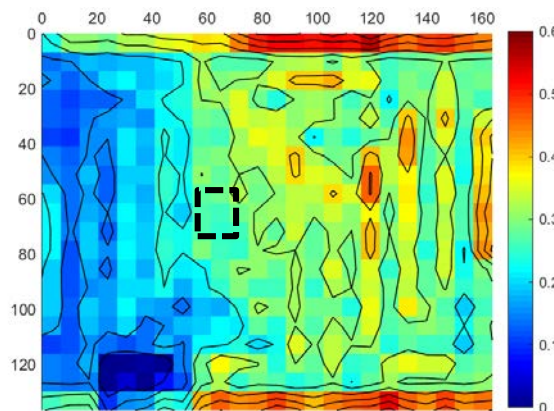
Validation of ageing via characterizations at BoT and EoT

Additional insights from
current density distribution
maps at 110 A



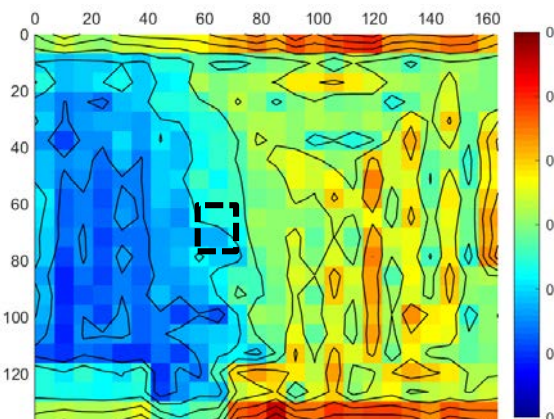
~ BoT (100 h REF cy)

REF
ID-FAST
DLC

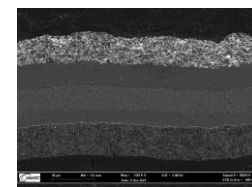


EoT

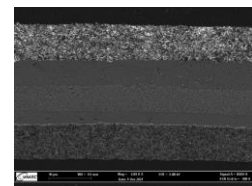
AST
F-stack
ID-FAST



Post mortem SEM

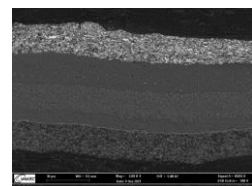


rib

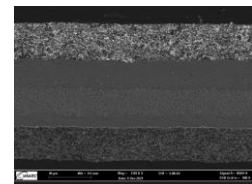


channel

→ To be further interpreted



rib



channel

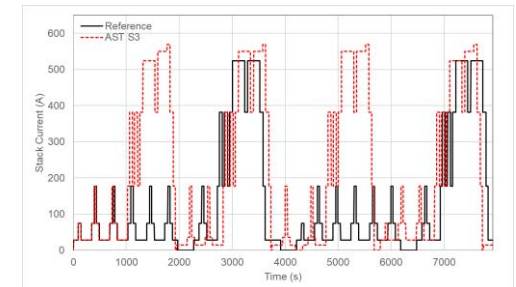
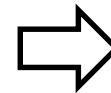
- ✓ Similar evolution
- ✓ With extended degraded zone at EoT AST

Some conclusions & next steps about AST approach for stacks

- ❑ AST based on exacerbated drive cycles
 - **First validation conducted on a stack**
 - Validation tests ongoing with other components (CCM B) on same stack design
 - **Further analyses regarding the correlation method between AST & REF**
 - Boundary conditions to be defined for valid application: minimum number of cycles to be applied or minimum duration; dependence on hardware design
 - **Parameters to be further considered: frequencies and amplitude of LP/HP pattern (reduced dwell times) and impact of current ramps**

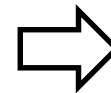
- ❑ Adaptation of AST approach to other stack platform (e.g. S3 300 cm²)

- **Possible adaptation of exacerbated load profiles to be assessed**



Example of possible adapted load profile

- **Specific profiles already proposed for the combined LP/HP AST cycles**



Next part of the presentation by ZSW

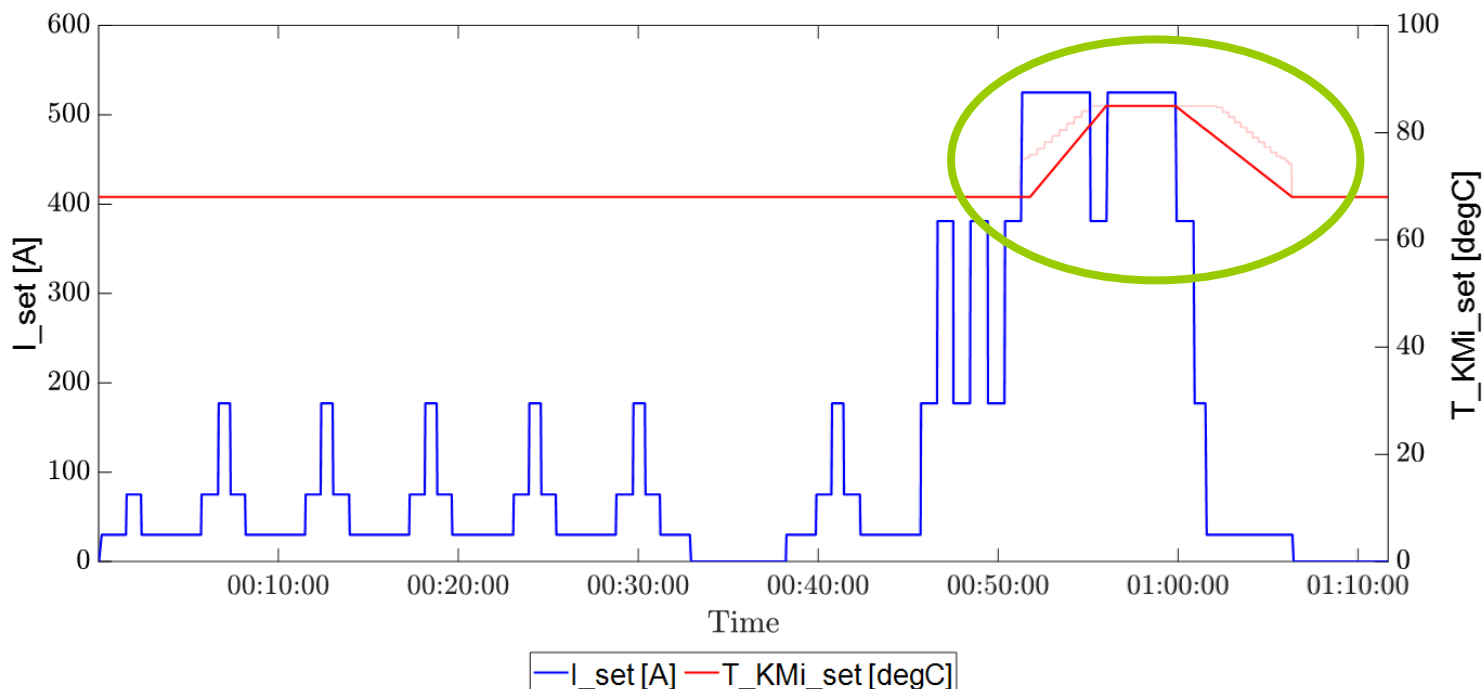
ID-FAST



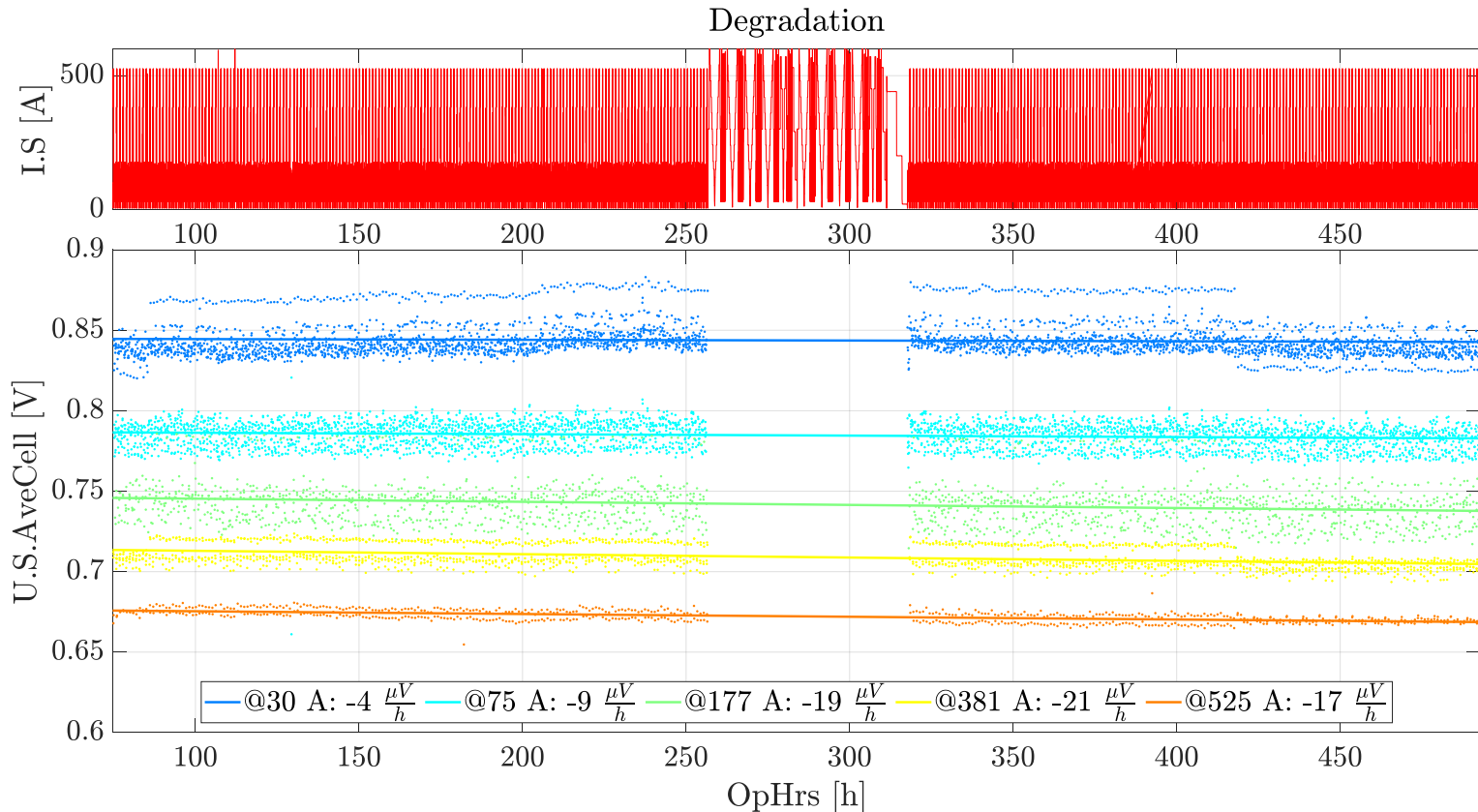
Reference and accelerated tests on S3 stacks

Improved implementation of load cycle for Durability Test

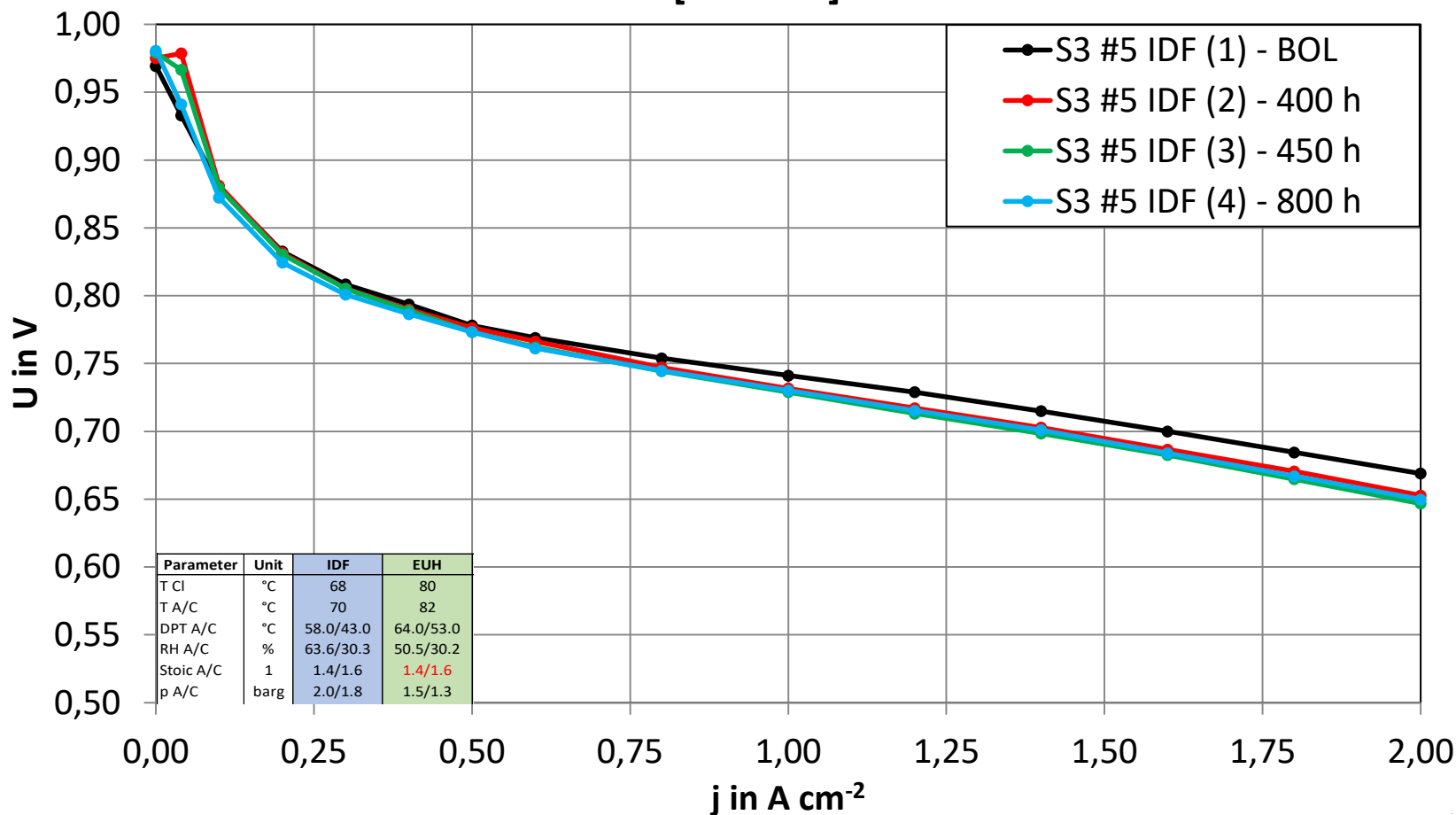
- ❑ New load cycle has a smooth temperature ramp and adapted holding times
- ❑ Total time per cycle (w/o stops): 3659 s ($\triangleq$ 60:59 min)
- ❑ Number of cycles: 325



□ Degradation rates of ID-FAST durability test



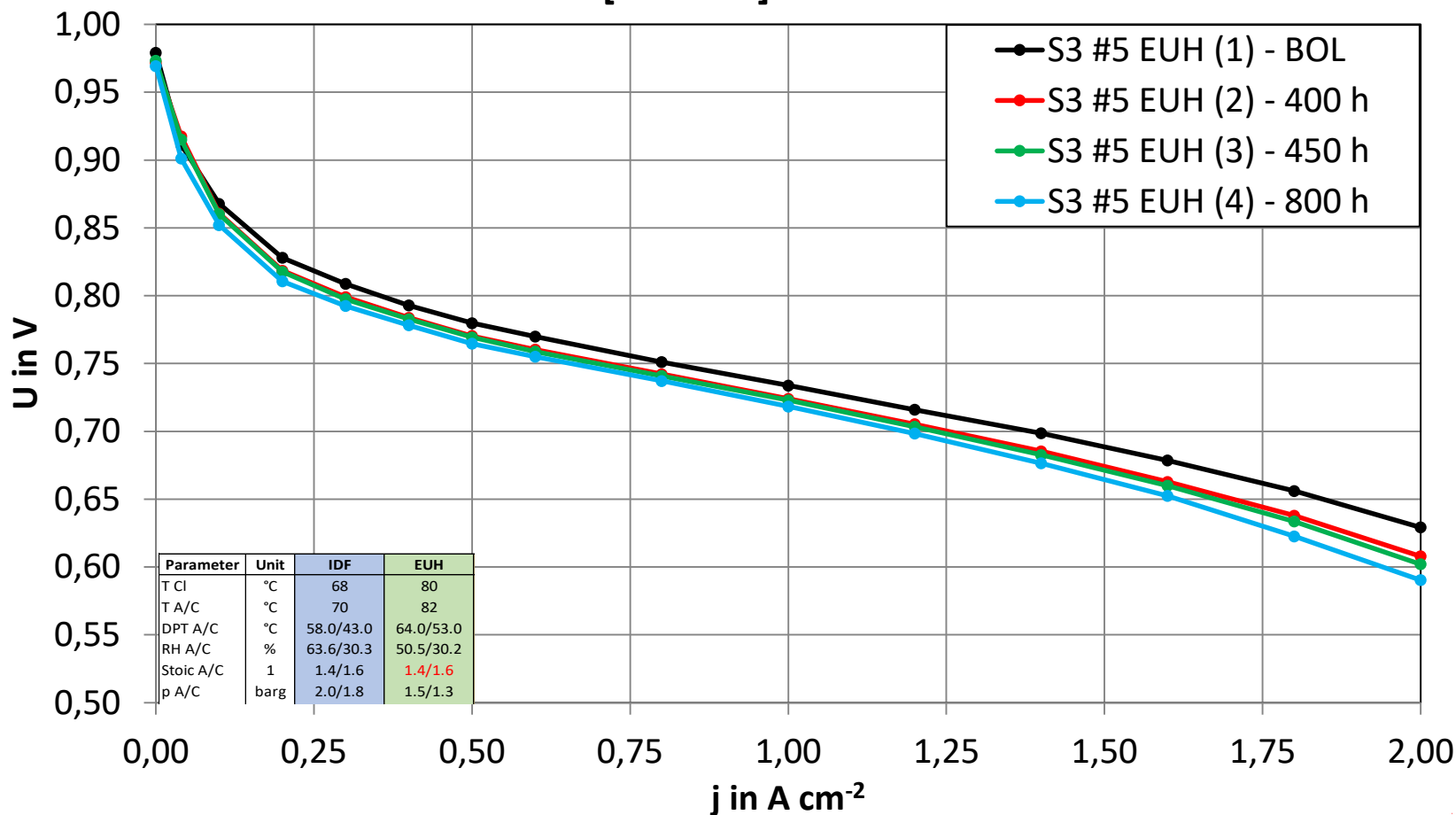
	@30 A	@75 A	@177 A	@381 A	@525 A	
Overall:	-4	-9	-19	-21	-17	$\mu V/h$
Per Cycle:	-4,1	-9,2	-19,3	-21,3	-17,3	$\mu V/cycle$

PowerCell S3 Stack #5 [300 cm²] - Overview ID-FAST

Time of recording given in calendar hours

Polarization Curves EU-Harmonized (CCM B, #2)

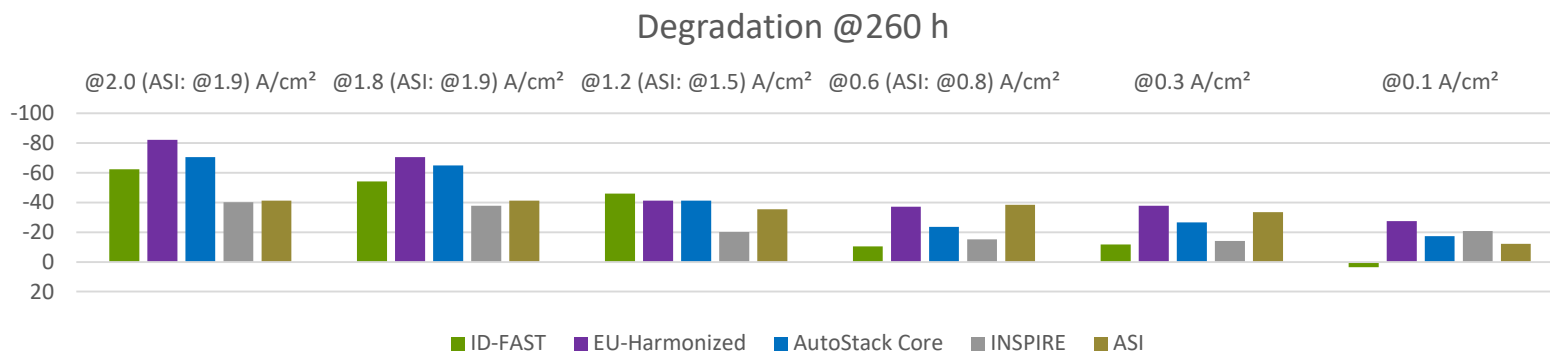
PowerCell S3 Stack #5 [300 cm²] - Overview EU-Harmonized



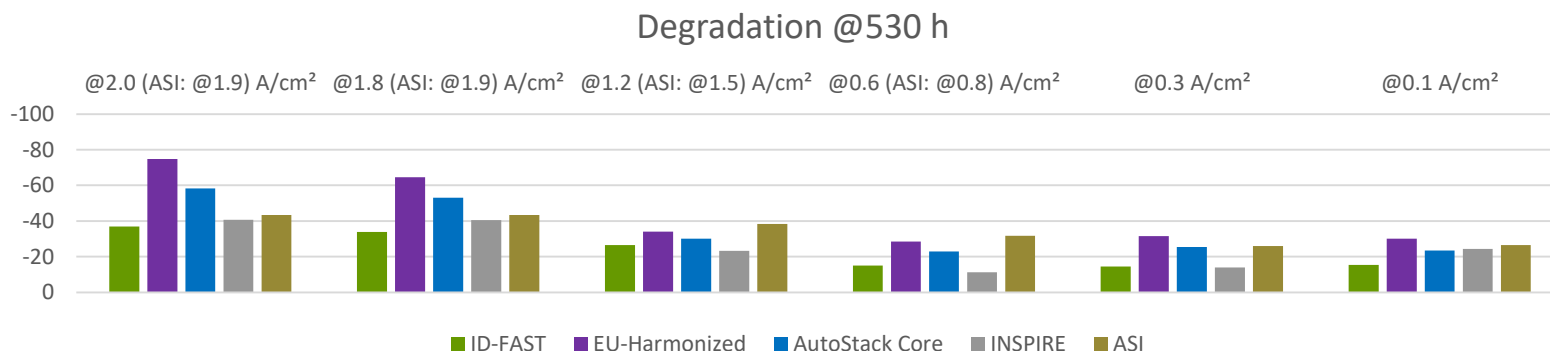
Time of recording given in calendar hours

Degradation rates from Polarization Curves (CCM B, #2)

□ Degradation rates obtained from polarization curves

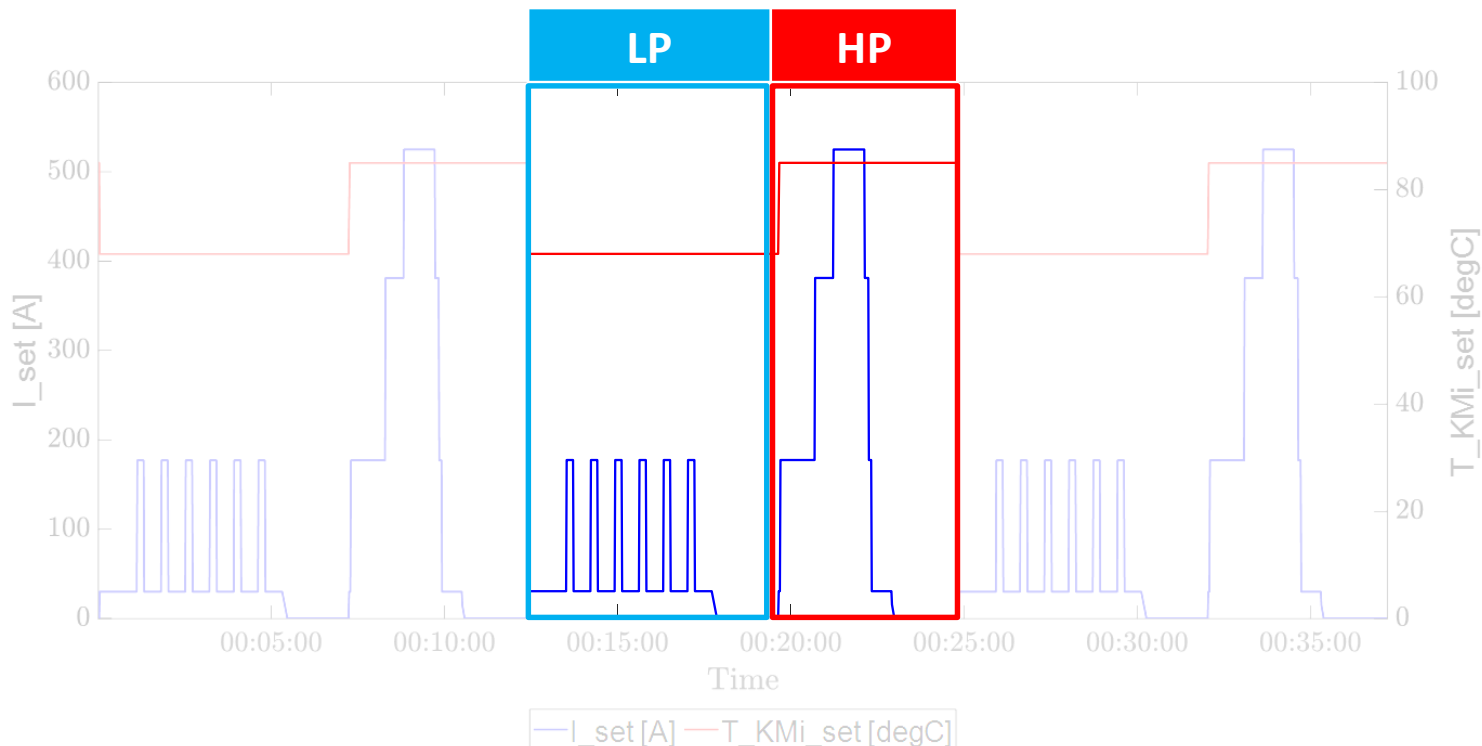


□ Initially higher degradation

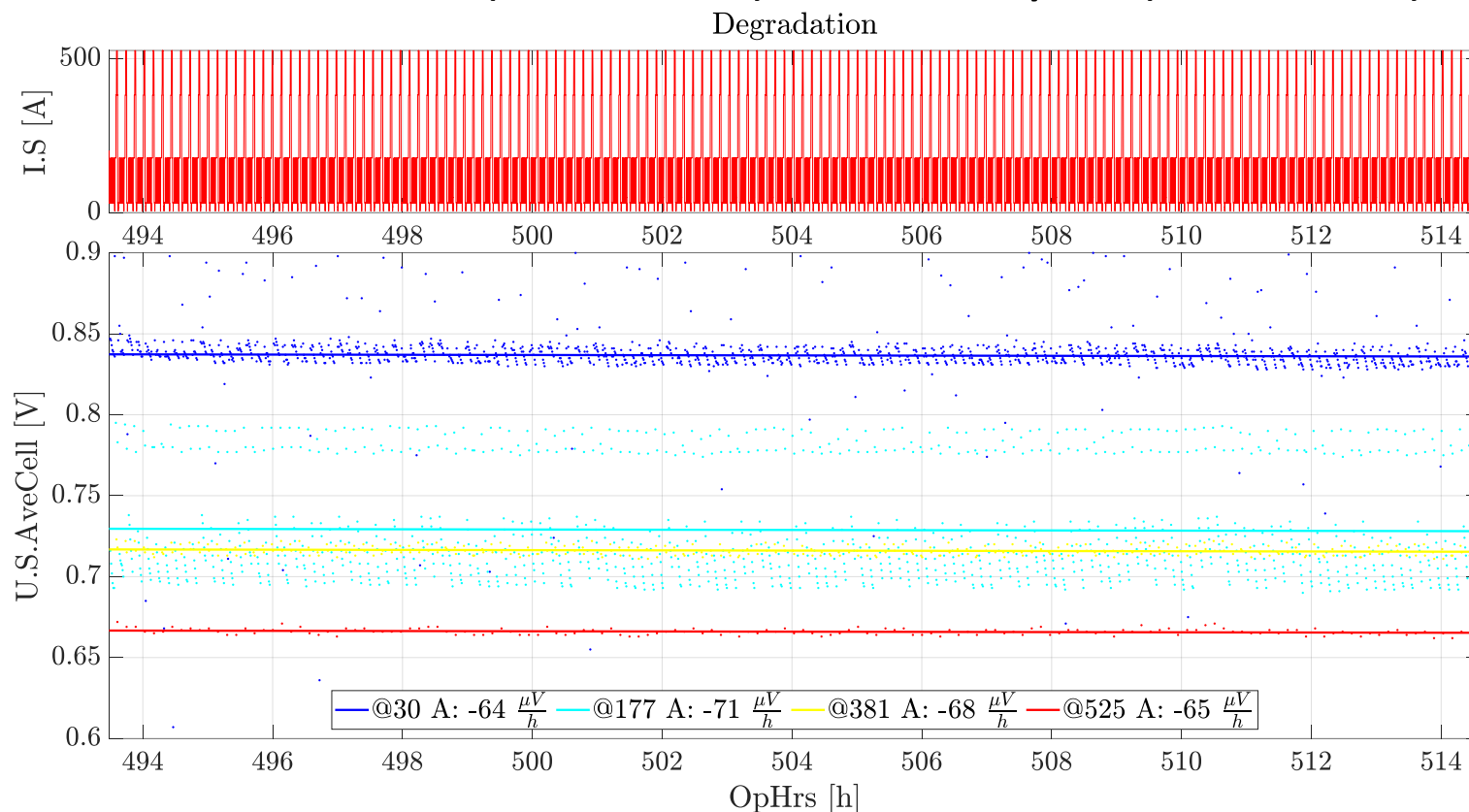


□ Clear stabilization effect for second set of POL curves

- ❑ Alternating Low- and High-Power ASTs separated by Stops
- ❑ Total time per cycle (w/o stops): 514 s ($\triangleq$ 08:34 min)
- ❑ Number of cycles: 150



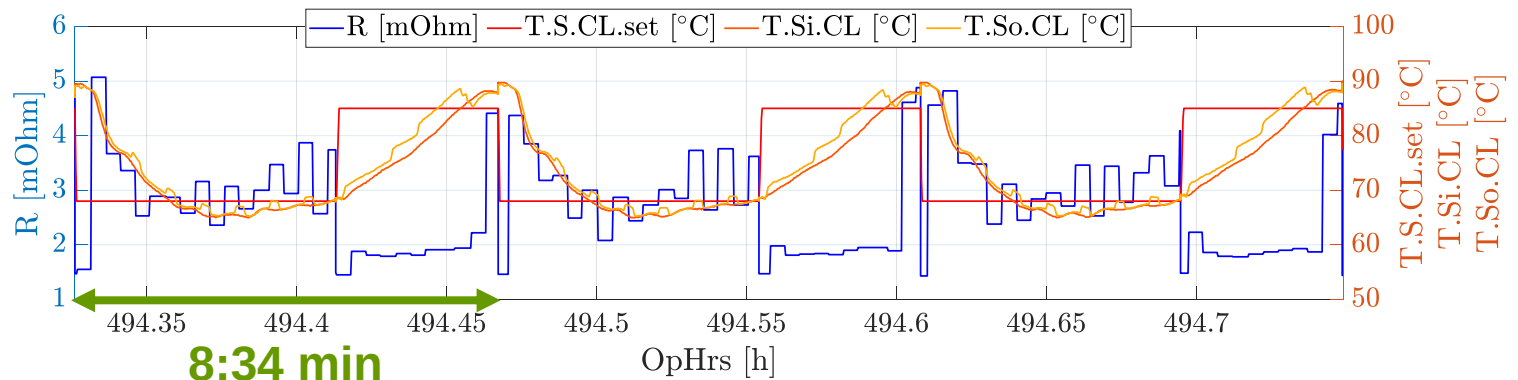
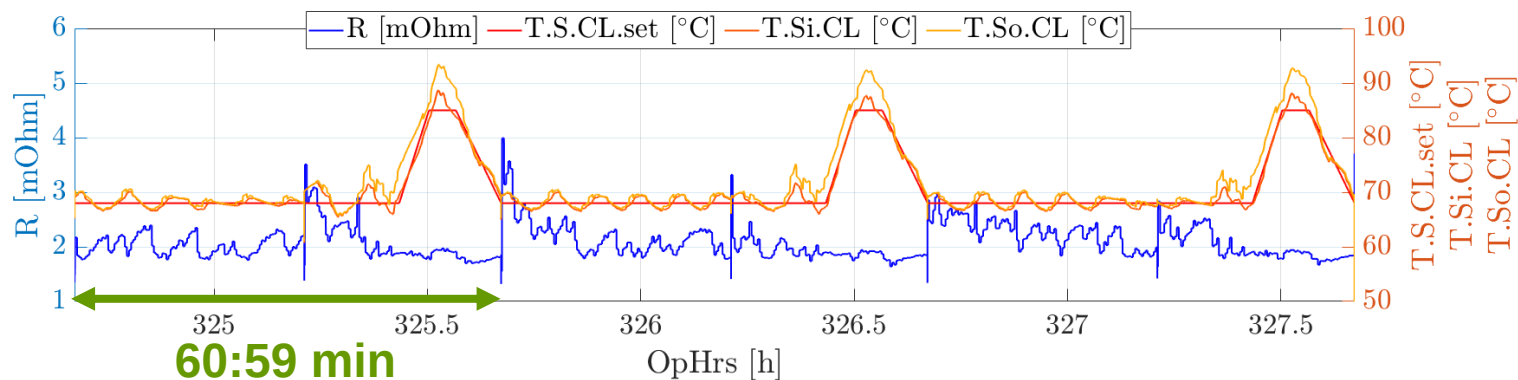
- 2 combined ASTs (17:08 min) $\approx$ 1 load cycle (60:59 min)



	@30 A	@ 177 A	@381 A	@525 A	
Overall:	-64	-71	-68	-65	$\mu V/h$
Per Cycle:	-9,0	-10,0	-9,6	-9,2	$\mu V/cycle$

HFR comparison between AST and durability test

- ❑ HFR in low- and high-power AST in part exacerbated compared to durability test
- ❑ Heating up and cooling down take comparatively longer due to the greater influence of the inertia of the system



- ❑ Reference durability test shows realistic degradation rates
 - **Order of magnitude is comparable to previous projects**

- ❑ Improved implementation of load cycle for reference durability test was tested successfully

- ❑ Low- and high-power AST successfully implemented on stack level
 - **Acceleration of degradation appears promising ($\approx 4x$ faster with reference to active time)**
 - **Further application complying to single cell test cycle is ongoing (200x LP / 200x HP)**
 - **Correlation factor will be further investigated**

Acknowledgements



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**THANK YOU FOR YOUR
ATTENTION**

